SPENSER D. GILLILAND

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OBJECTIVE

- Further develop skillset in heterogeneous compute technologies
- Specific interest in FPGA/ASIC and performance tuning using high level synthesis
- Jointly develop large scale systems that are on the cutting edge of advanced technologies

SKILLS

Software

Embdedded: Buildroot Linux, LynxOS/SE/178
Server: Debian/Ubuntu/Red Hat/Fedora
Development: C/C++, OpenCL/CUDA, Python, Linux Kernel
Build: Autotools, Cmake, KConfig, GDB
Server: OpenStack, SQL, LDAP, Jenkins, Git, Puppet, MPI

Hardware

Schematic & Layout: Mentor Design Suite, Cadence Allegro, gEDA suite, Eagle
Signal Integrity: Hyperlynx, ICX, IBIS
FPGA/ASIC: VHDL, Verilog, Vivado HLS, Impulse C, IPI, Chip Scope, Modelsim
Processors: ARM, PPC, X86, Microblaze
SoC: TI OMAP3/4/5, TI am335x, I.MX6, Zynq, Allwinner, Microblaze

EXPERIENCE

Xilinx, San Jose, CA
Senior Software Engineer Summer 2014-present

- Drive development of Vivado HLS and OpenCL technologies
- Provide technical guidance and development for $10M+ LTR accounts
- File three patents that are currrently pending
- Develop math builtins in HLS C, resulting in OpenCL conformance submission
- Create several open source samples: Convolve, SHA1, Bitcoin Mining, Nearest Neighbor, Histogram
- Implent internal OpenStack cluster and create images for SuperVessel/Nimbix/VirualBox/Docker

Embedded Computing and Signal Processing Lab, Chicago, IL
Lab Leader 2012-present

- Code signal processing algorithms using hardware/software co-design
- Implement Linux based operating system for Microblaze soft-core processor and Zynq All Programable System-on-Chip
- Manage computing resources and configure project management applications

Research Assistant 2010-2012

- Develop signal processing platform based on high speed ADC/DAC and Xilinx Virtex 5 FPGA with custom peripherals utilizing Xilinx EDK
- Create VHDL and Verilog source code for custom peripherals using AXI and PLB bus

Google, http://www.google-melange.com/
Summer of Code Internship - Build Root Summer 2013

- Mainline over 50+ patches including GPU, and Video Decode support for the open source project Buildroot http://buildroot.org
- Add support for ARM Mali, PowerVR, and Vivante graphical processing units (GPU)
- Hands on experience with TI OMAP, TI335x, I.MX6, Allwinner, and Raspberry Pi ARM based systems

Reconfigurable Computing Project, Waco, TX
Research Assistant 2008-2010
- Created a cluster of MPI nodes running Debian Linux on Xilinx FPGA
- Gained competency with Xilinx ISE and EDK development tools
- Assisted with the implementation of Impulse C high level synthesis accelerators
- Developed kernel drivers and RFS for Debian Linux

Raytheon Company, McKinney, TX
Operations Intern Summer 2010
- Tested an L2 GPS upgrade to the Multi-spectral Targeting System (MTS)
- Gained valuable insight into the fields of camera sensor technology and GPS

Research and Development Intern Summers 2009, 2010
- Verified Xilinx Virtex 5 FPGA firmware for High Speed IO subsystem
- Wrote Linux drivers for firmware and integrated into Gentoo BSP
- Created board level tests for a multi-chip DSP subsystem

Signal Integrity Intern Summer 2009
- Specified and verified compliance of routing rules using ICX and HyperLynx
- Ran signal integrity evaluations in HyperLynx and presented findings in formal reviews
- Used scripting experience to create routing rules in half the time with greater accuracy

LynuxWorks Inc., San Jose, CA
Integration and Test Intern 2008-2009
- Developed test suites for LynxSecure, a security enhanced embedded hyper-visor
- Documented testing procedures to maintain ISO 9000

Systems Engineering Intern Summer 2007
- Gained proficiency in LynuxWorks embedded Linux and UNIX product lines
- Developed and implemented a virtual lab for systems engineers utilizing OpenVPN
- Performed installation and configuration on ARM, MIPS, x86, PPC, and Xilinx FPGA

EDUCATION

Illinois Institute of Technology (IIT) - Chicago, IL
Ph.D. Computer Engineering 2012-present
- Research Interest: FPGA based Reconfigurable Computing for High Speed Signal Analysis

M.S. Computer Engineering 2010-2012
- Concentration: Computer Hardware Design

Baylor University - Waco, TX
B.S. Electrical and Computer Engineering 2006-2010
- Mathematics Minor

AWARDS

2013 International Ultrasonics Symposium Student Paper Competition, First Place Winner
"Performance Evaluation of FPGA Based Embedded ARM Processor for Ultrasonic Imaging"
- Obtained travel support to attend conference in Prague, Czech Republic
- Choosen from amongst over 200 participants

2013 Illinios Institute of Technology Poster Competition, Finalist
"Reconfigurable Ultrasonic System-On-Chip Hardware (RUSH)"
- One of two students choosen to represent the Electrical and Computer Engineering department in this campus wide event

PUBLICATIONS

Submitted Paper - S. Gilliland and J. Saniie, "Architecture of the reconfigurable ultrasonic system-on-chip hardware platform." July 2013

Accepted Paper - W. Yi, S. Gilliland, and J. Saniie, "Wireless sensor network for structural health monitoring using system-on-chip with android smartphone." August 2013

Accepted Paper - W. Yi, S. Gilliland, and J. Saniie, "Mobile ultrasonic signal processing system using android smartphone." August 2013

Published Paper (in print) - P. Govindan, T. Gonnot, S. Gilliland, and J. Saniie, "3d ultrasonic signal compression algorithms for high signal fidelity." August 2013

Published Paper (in print) - **Student Paper Competition 1st Place** - S. Gilliland, P. Govindan, T. Gonnot, and J. Saniie, "Performance evaluation of fpga based embedded arm processor for ultrasonic imaging." July 2013

Published Paper (in print) - P. Govindan, S. Gilliland, T. Gonnot, and J. Saniie, "Hw/sw co-design for reconfigurable ultrasonic system-on-chip platform." February 2013

Published Paper - P. Govindan, S. Gilliland, T. Gonnot, and J. Saniie, "Reconfigurable ultrasonic system-on-chip hardware (rush) platform for real-time ultrasonic imaging applications," in *Ultrasonics Symposium (IUS), 2012 IEEE International*, pp. 463–466, 2012 - `http://dx.doi.org/10.1109/ULTSYM.2012.0115`

Published Paper - P. Govindan, S. Gilliland, A. Kasaeifard, T. Gonnot, and J. Saniie, "Performance analysis of reconfigurable ultrasonic system-on-chip hardware platform," in *Instrumentation and Measurement Technology Conference (I2MTC), 2013 IEEE International*, pp. 1550–1553, 2013 - `http://dx.doi.org/10.1109/I2MTC.2013.6555674`

Invited Book Chapter - J. Saniie, E. Oruklu, S. Gilliland, and S. Aslan, "Reconfigurable Ultrasonic Smart Sensor Platform for Nondestructive Evaluation and Imaging Applications", S. Nihtianov and A. Estepa, *Smart Sensors and MEMS: Intelligent Devices and Microsystems for Industrial Applications*. Woodhead Publishing Limited, 2013 - `http://www.woodheadpublishing.com/en/book.aspx?bookID=2580`

Published Paper - S. Gilliland, J. Saniie, and S. Aslan, "Linux based reconfigurable platform for high speed ultrasonic imaging," in *Circuits and Systems (MWSCAS), 2012 IEEE 55th International Midwest Symposium on*, pp. 486 –489, aug. 2012 - `http://dx.doi.org/10.1109/MWSCAS.2012.6292063`

Master's Thesis - S. Gilliland, "System-on-chip for research in ultrasonic signal processing and imaging applications," Master's thesis, Illinois Institute of Technology, 2012 - `http://hdl.handle.net/10560/2842`

REFERENCES

Available upon request